What is claimed is:

1. A method of filtering over-sampled data comprising:
   a. receiving a word of over-sampled data including a plurality of sample bits for each of a plurality of data bits;
   b. detecting a sample bit having one logic value and, on either side of it, bits having the opposite logic value; and
   c. outputting the received word with the sample bit having said one logic value inverted.

2. The method of claim 1 wherein said step of detecting comprises:
   a. exclusively ORing each sample bit in said word separately with the next highest and next lowest bits; and
   b. ANDing the results said ORing.

3. The method of claim 2 and further including providing a history bit to supply the next highest bit for the most significant bit of said word.

4. The method according to claim 3 wherein a plurality of words in succession are received, with the steps of claim 1 performed for each word, and further including saving the least significant bit of a last previous word received as the history bit for the next word received.

5. The method according to claim 4 comprising receiving words until the end of a packet is reached.

6. The method of claim 2 wherein said step of outputting comprises outputting each of said sample bits uninverted if the result of said ANDing is one logic level and inverted if the result is the other logic level.

7. The method according to claim 1 comprising receiving said word from an over-sampler.

8. The method according to claim 7 and further comprising selecting a word to be received from between two over-samplers.

9. The method according to claim 1 wherein said over-sampled data is USB 2.0 data.

10. Apparatus for filtering over-sampled data comprising:
    a. detection logic coupled to receiving a word of over-sampled data including a plurality of sample bits for each of a plurality of data bits and to detect a sample bit having one logic value and on either side of it, bits having the opposite logic value; and
    b. an output circuit outputting the received word with the sample bit having said one logic value inverted.

11. The apparatus of claim 10 wherein said detection logic comprises:
    a. a plurality of terminals for receiving said sample bits for each of a plurality of data bits;
    b. a plurality of first two input logic circuits to perform an exclusive OR function, each having its inputs coupled to two adjacent terminals; and
    c. a plurality of second two input logic circuits to perform an AND function, each having as inputs outputs of two adjacent first logic circuits.

12. The apparatus of claim 11 and further including a storage element to store a history bit, an output of said storage element coupled to one of said first logic circuits having as a second input a sample bit which is most significant.

13. The apparatus of claim 12 wherein said output circuit comprises:
    a. a plurality of inverters, one coupled to each terminal; and
    b. a plurality of multiplexers, each having a first data input coupled to an output of one of said inverters, an second data input coupled to the corresponding terminal, and a control input coupled to the output of the one of said second logic circuits associated with said terminal and an output.

14. The apparatus of claim 13 wherein a plurality of words in succession are to be received, said storage element having an input coupled to the least significant sample bit and having a clock input to clock said input to its output prior to receiving a new word.

15. The apparatus of claim 14 and further comprising an over-sampler to supply said words to said terminals.

16. The apparatus of claim 15 wherein two over-samplers are provided and further including a selection circuit to select between two over-samplers.

17. The apparatus of claim 16 wherein said selection circuit is a multiplexer.

18. The apparatus of claim 13 wherein said over-sampled data is USB 2.0

19. A computer readable memory containing program instructions that, when executed by a processor, cause the processor to:
    a. receive a word of over-sampled data including a plurality sample bits for each of a plurality of data bits;
    b. detect a sample bit having one logic value and, on either side of it, bits having the opposite logic value; and
    c. output the received word with the sample bit having said one logic value inverted.

20. A computer readable memory according to claim 19 wherein said processor is caused to

a. exclusively OR each sample bit in said word separately with the next highest and next lowest bits; and

b. AND the results said exclusive Oring.

21. A computer readable memory according to claim 20 wherein said processor is caused to provide a history bit to supply the next highest bit for exclusive ORing with the most significant bit of said word.

22. A computer readable memory according to claim 21 wherein said processor is caused to receive a plurality of words in succession, with the steps of claim 1 performed for each word and said processor is further caused to save the least significant bit of a last previous word received as the history bit for the next word received.

23. A computer readable memory according to claim 22 wherein said processor is caused to receive words until the end of a packet is reached.

24. A computer readable memory according to claim 23 wherein said processor is caused to output said each sample bits uninverted if the result of said ANDing is one logic level and inverted if the result is the other logic level.

25. A computer readable memory according to claim 21 wherein said over-sampled data is USB 2.0 data.